HIGH EFFICIENCY HARMONIC CONTROL AMPLIFIER

Bernhard Ingruber, Werner Pritzl, and Gottfried Magerl

Department of Communications and Radio-Frequency Engineering
Vienna University of Technology
Gusshausstrasse 25/389, A-1040 Vienna, Austria

ABSTRACT

A new high efficiency amplifier concept which ideally delivers 100 % drain efficiency and class A gain is described. The power amplifier realized with a commercially available GaAs FET has demonstrated 74 % power-added efficiency, 27.9 dBm output power, and 14.4 dB gain at 1.62 GHz.

INTRODUCTION

The improvement of power-added efficiency and reliability of microwave power amplifiers has been investigated by many researchers over the last twenty-five years (Table 1). Most practical realizations of high efficiency microwave power amplifiers make use of the so called class F mode, where the device is biased at class B or class B near class AB and harmonics are controlled in such a way that the device output voltage becomes rectangular [1]-[5] (Fig.1). Many modifications of this switched type amplifier have been introduced by several designers to improve the efficiency, e.g., class E [6], rectangularly driven class B (rB) [7], [8], or harmonic reaction amplifier (HRA) [9], [10]. All of them operate at a class B near input level, where up to half of the input power is lost. This affects the gain which is about 3 to 6 dB less than the corresponding class A gain and, therefore, the power-added efficiency is decreased drastically as compared with the high device efficiency. Furthermore, device reliability is limited due to high negative gate to source voltage [11].

In this work we present an innovative amplifier concept which combines the advantage of high gain of class A with the advantage of high drain efficiency of class F.

Ref.	Class	f [GHz]	P_{OUT} [dBm]	G_T [dB]	η_D [%]	η_{PA} [%]
[1]	F	1.75	24.5	11.0	77	71
[2]	F	0.9	35.7	12.7	56	53
[3]	F	0.84	32.0	-	76	-
[4]	F	1.7	31.8	11.8	73	68
[5]	F	0.9	33.0	11.0	76	70
[6]	E	1.0	29.7	14.7	75	73
[7]	rB	0.9	36.1	13.0	63	60
[8]	rB	0.8	36.2	12.2	66	62
[9]	HRA	2.0	37.0	12.0	75	70
[10]	HRA	1.7	34.1	9.0	86	75

Table 1 Comparison of achievements in high efficiency power amplifier design reported in the literature.

CONCEPT

The amplifier concept that we describe is based on a modified class A amplifier that uses a half sinusoidal input signal to operate the transistor as a switch (Fig.1). With the suitable har-

WE 3F

0-7803-3246-6/96/$5.00 © IEEE

monic load the amplifier offers the same drain efficiency as a class F amplifier (ideally 100 %), but with the gain of class A. Consequently, power-added efficiency of this half sinusoidally driven class A harmonic control amplifier (hHCA) is higher compared with class F. Reliability is expected to be improved, too, as the gate of the device is stressed much less due to reduced input power and lower negative input voltage.

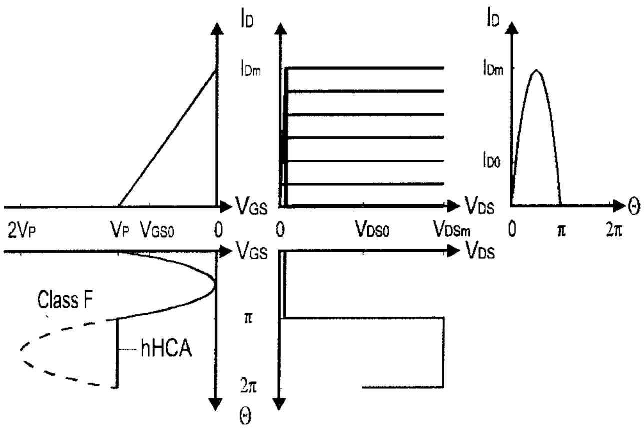

Fig.1 Comparison of ideal waveforms and load lines of class F and hHCA.

The desired input signal is generated by a pulse shaping stage which operates as a resistively loaded class B amplifier and needs not to be overdriven. This promotes the amplifier reliability, too. Due to the high gain of the power stage the reduction of overall efficiency due to the driver stage is kept within a few percents, and this justifies the introduction of this two-stage hHCA concept.

DESIGN

Fig.2 illustrates the block diagram of the two-stage amplifier where the half sinusoidal signal is approximated by the fundamental frequency along with the second harmonic. At the driver FET output fundamental and second harmonic signal are separated from each other by an appropriate filtering network. With two continuously variable attenuators and a continuously variable phase shifter ($\varphi(f_0)$ = 0...180°) the optimum input signal can be adjusted at the gate of the power FET after combining both signal paths. When magnitude and phase relation of both input signals of the power amplifier are known, the operation condition of the driver amplifier is changed for this optimum fundamental and second harmonic output power and the tuning network can be replaced by simple transmission lines.

In order to separate fundamental and second harmonic frequency signal we constructed a frequency splitting network as illustrated in Fig.3. A detailed analysis of this circuit shows that all odd harmonics are guided to the fundamental frequency output, whereas all even harmonics are guided to the output of the second harmonic. Based on this circuit we were able to control the impedance matching of the first three harmonics at the driver amplifier output and the power amplifier input independently.

At the driver amplifier input a tuneable second harmonic source impedance matching was foreseen to optimize its fundamental to second

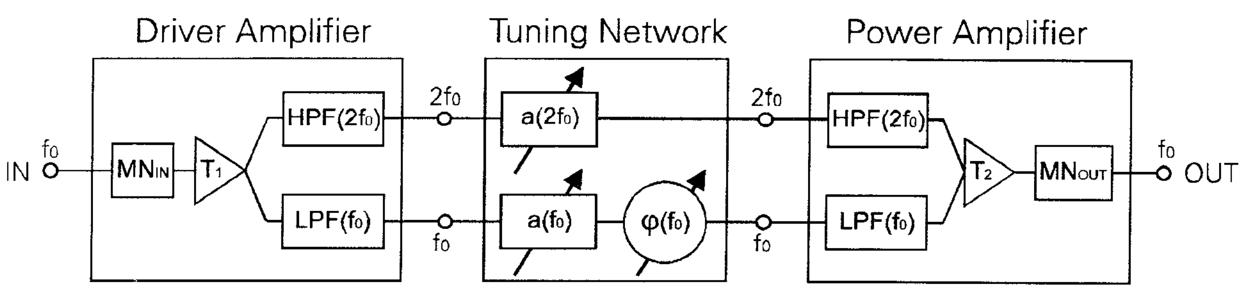

Fig.2 Block diagram of the two-stage hHCA with tuning network.

harmonic output power ratio. At the power stage output we implemented tuneable stubs to control second and third harmonic load impedances which were crucial for an optimum drain pulse shaping and, therefore, for maximum power-added efficiency. Furthermore, fundamental frequency and second harmonic input matching of the power amplifier could be improved via variable tuning stubs, too.

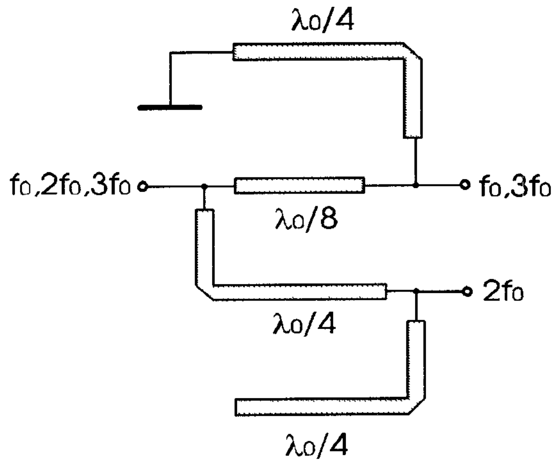

Fig.3 Frequency splitting network. Lengths of lines are given in wavelengths of fundamental frequency.

The transistor that we used for the development of a hybrid version of both driver and power stage of an hHCA at 1.62 GHz was a commercially available packaged GaAs FET (Thomson TC6519). For our simulations with JOmega™ [12] we have generated a large signal model of this FET with the parameter extraction software HarPE™ [13]. Therefore, we had to perform DC and multiple bias S-parameter measurements (up to 10 GHz) using a fully automatic computer controlled transistor characterization unit developed by us.

PERFORMANCE

The first realizations of driver and power amplifier operated optimally with only little tuning at the specified stubs. Therefore, no redesigns had to be performed and the amplifier had been fully designed on the circuit simulator.

The measured output power and power-added efficiency characteristics of the power amplifier stage are shown in Fig.4. It had demonstrated 74 % power-added efficiency, 27.9 dBm output power, and 14.4 dB gain at 1.62 GHz which was well in agreement with the simulation results (Table 2). Furthermore, this was an increase of 3 % power-added efficiency, 1.1 dB output power, and 3 dB gain as compared with the power stage with the same FET operated at class F (Table 3).

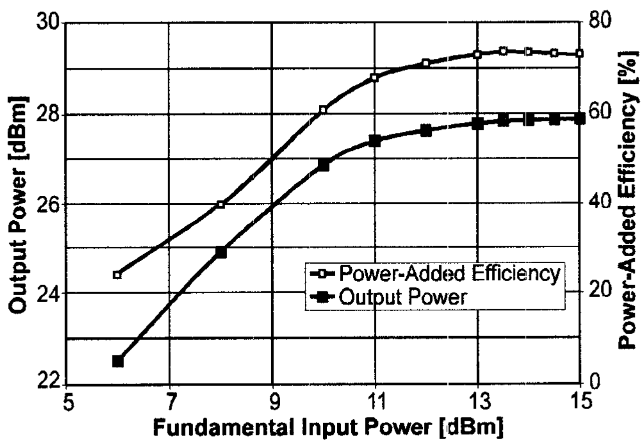

Fig.4 Measured output power and power-added efficiency versus fundamental input power of half sinusoidally driven power amplifier at 1.62 GHz and $P_{IN}(1)/P_{IN}(2) = 6.5$ dB.

Power Amplifier	P_{OUT} [dBm]	G_T [dB]	η_D [%]	η_{PA} [%]	$P_{IN}(1)/P_{IN}(2)$ [dB]
Simulation	28.2	15.1	79	76	7.8
Realization	27.9	14.4	77	74	6.5

Table 2 Comparison of simulation and measurement of half sinusoidally driven power amplifier at 1.62 GHz.

Power Amplifier	P_{OUT} [dBm]	G_T [dB]	η_D [%]	η_{PA} [%]	$P_{IN}(1)/P_{IN}(2)$ [dB]
hHCA	27.9	14.4	77	74	6.5
Class F	26.8	11.4	77	71	-

Table 3 Comparison of measured performance of hHCA and class F amplifier at 1.62 GHz.

The combination of driver and power amplifier without tuning network delivered 71 % overall efficiency, 27.9 dBm output power, and 22.4 dB gain.

CONCLUSION

An innovative high efficiency harmonic control amplifier concept where the power stage is driven by a half sinusoidal signal delivers high power-added efficiency along with class A gain. The realization of such a power amplifier at 1.62 GHz has demonstrated 74 % power-added efficiency, 27.9 dBm output power, and 14.4 dB gain.

ACKNOWLEDGEMENT

We would like to thank F.A. Petz and M. Pfurtscheller for their technical supports throughout this research project. This work was performed within an ESA project in co-operation with Hirschmann (Austria).

REFERENCES

[1] C. Duvanaud, S. Dietsche, G. Pataut, J. Obregon: "High-efficient class F GaAs FET amplifiers operating with very low bias voltages for use in mobile telephones at 1.75 GHz." IEEE Microwave and Guided Wave Letters, Aug. 1993, vol. 3, no. 8, p. 268-270.

[2] M. Easton, R. Basset, D.S. Day, C. Hua, C.S. Chang, J. Wel: "A 3.5 watt high efficiency GaAs FET Amplifier for digital telephone communications." IEEE MTT-S International Microwave Symposium Digest, 1992, vol. 3, p. 1183-1184.

[3] J.E. Mitzlaff: "High efficiency RF power amplifier." United States Patent, 5. Jan. 1988, Patent Number: 4,717,884.

[4] T. Nojima, S. Nishiki, K. Chiba: "High-efficiency quasimicrowave GaAs FET power amplifier." Electronics Letters, 7 May 1987, vol. 23, no. 10, p. 512-13.

[5] K. Chiba, N. Kanmuri: "GaAs FET power amplifier module with high efficiency." Electronics Letters, 24 Nov. 1983, vol. 19, no. 24, p. 1025-6.

[6] T.B. Mader, Z.B. Popovic: "The transmission-line high-efficiency class-E amplifier." IEEE Microwave and Guided Wave Letters, Sept. 1995, vol. 5, no. 9, p. 290-292.

[7] S. Toyoda: "High efficiency single and push-pull power amplifiers." IEEE MTT-S International Microwave Symposium Digest, 1993, vol. 1, p. 277-80.

[8] S. Toyoda: "High efficiency amplifiers." IEEE MTT-S International Microwave Symposium Digest, 1994, vol. 1, p. 253-56.

[9] T. Nojima, S. Nishiki: "High efficiency microwave harmonic reaction amplifier." IEEE MTT-S International Microwave Symposium Digest, 1988, vol. 2, p. 1007-10.

[10] S. Nishiki, T. Nojima: "Harmonic reaction amplifier - a novel high-efficiency and high-power microwave amplifier." IEEE MTT-S International Microwave Symposium Digest, 1987, vol. 2, p. 963-966.

[11] J.V. DiLorenzo, D.D. Khandelwal: "GaAs FET principles and technology". Artech House, Dedham, Massachusetts, 1982.

[12] Hewlett Packard: "JOmega™ - Series 4 - Version 5." HP-EEsof, Feb. 1994.

[13] OSA: "HarPE™ - Version 1.8." Optimization Systems Associates Inc., P.O. Box 8083, Dundas, Ontario, Canada L9H 5E7.